



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#8
WM
5/22/03

Docket No.: CYPR-CD00055

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit.

Date of Deposit:	05/08/03	Name of Person Making the Deposit:	ANTHONY CHOU	Signature of the Person Making the Deposit:	<i>Anthony Chou</i>
------------------	----------	------------------------------------	--------------	---	---------------------

Inventor(s): James Daniel Merchant, Gordon Carsksdon, Brian P. Evans, Jeffrey Scott Hunt, Anup Nayak and Andrew Wright

Serial No.: 09/684,160

Group Art Unit: 2172

Filed: 10/04/00

Examiner: Hamilton, M. G.

Confirmation No:

Title: METHOD AND SYSTEM FOR GENERATING A BIT ORDER DATA STRUCTURE OF CONFIGURATION BITS FROM A SCHEMATIC HIERARCHY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

TRANSMITTAL OF FORMAL DRAWINGS

In response to Drawing Informalities

attached please find:

☒ (a) the formal drawings for this application
Number of Sheets 16

X Each sheet of drawing indicates the identifying indicia suggested in § 1.84(c) on the reverse side of the drawing

☐ (b) a copy of the NOTICE OF INFORMAL DRAWINGS

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 5/8/03

By: *Ronald M. Pomeranke*
Ronald M. Pomeranke
Reg. No. 43,009

RECEIVED
MAY 13 2003
Technology Center 2100

APPROVED O.G. FIG
CLASS. SUBCLAS
INVENTOR(S): James Daniel Merchant, Gordon Carskadon, Brian P. Evans, Jeffrey Scott Hunt, Anup
Nayak, Andrew Wright
USSN: 09/684,160 ATTORNEY DOCKET #: CYPR-CD00055

Q I P E
MAY 08 2003
PATENT & TRADEMARK OFFICE

TITLE: METHOD AND SYSTEM FOR GENERATING A BIT ORDER DATA STRUCTURE OF
CONFIGURATION BITS FROM A SCHEMATIC

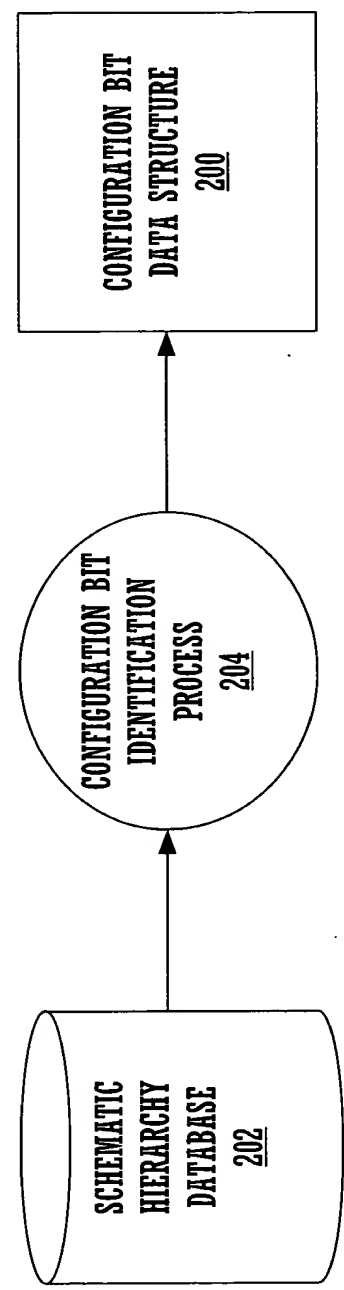
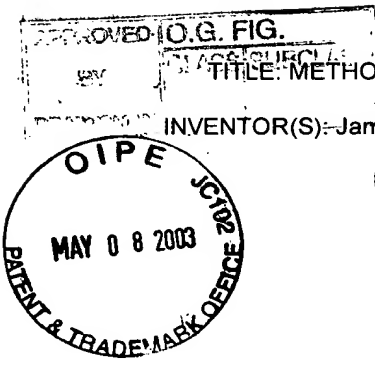


FIGURE 1A



200

"libraryName1/Cellname1"				
id:	wordLine 220	bitLine 222	Logical Name 224	Instance Path 226
data:	w/<0>	b/<0>	mc<0>/c<0>	"top" "memory" "inst3" "mc<0>" "inst18" "c<0>"
	w/<0>	b/<10>	mc<0>/c<10>	"top" "memory" "inst3" "mc<0>" "inst42" "c<0>"

"libraryName1/Cellname2"				
id:	wordLine 220	bitLine 222	Logical Name 224	Instance Path 226
data:	w/<10>	b/<0>	mc<0>/c<0>	"top" "memory" "inst5" "mc<0>" "inst8" "c<0>"

FIGURE 1B

INVENTOR(S): James Daniel Merchant, Gordon Carskadon, Brian P. Evans, Jeffrey Scott Hunt, Anup
Nayak, Andrew Wright

USSN: 09/684,160 ATTORNEY DOCKET #: CYPR-CD00055

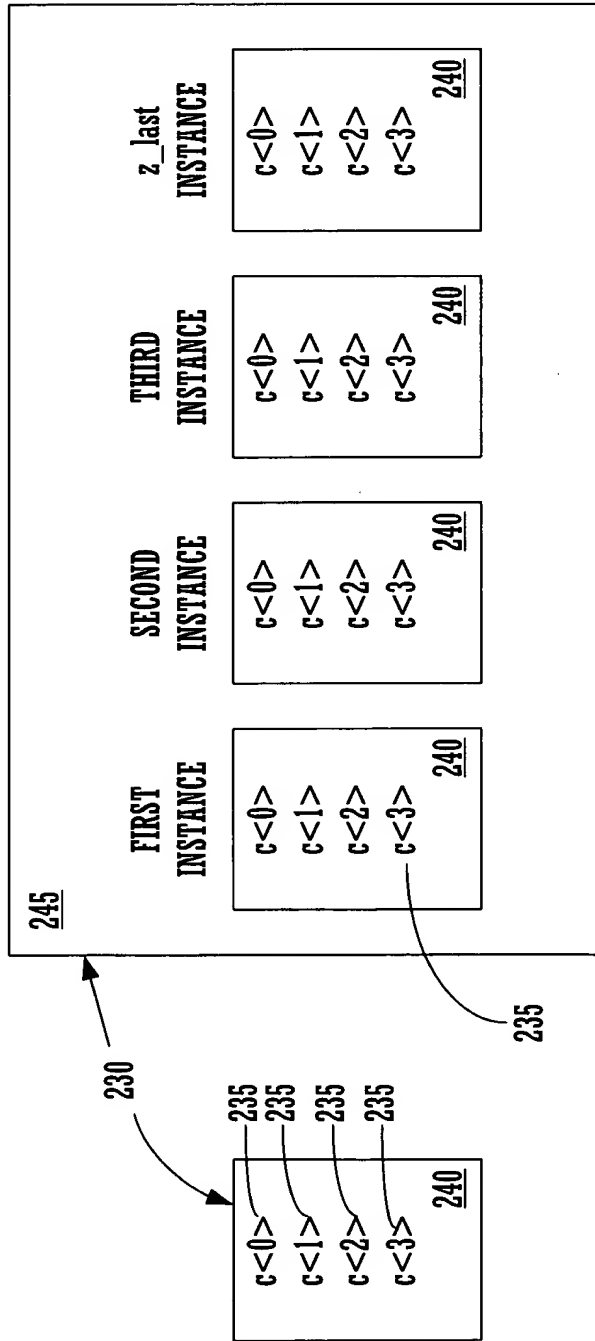


FIGURE 2A

APPROVED 0.3 FIG.
CLASSIFICATION

TITLE: METHOD AND SYSTEM FOR GENERATING A BIT ORDER DATA STRUCTURE OF CONFIGURATION BITS FROM A SCHEMATIC

INVENTOR(S): James Daniel Merchant, Gordon Carskadon, Brian P. Evans, Jeffrey Scott Hunt, Anup Nayak, Andrew Wright

USSN: 09/684,160 ATTORNEY DOCKET #: CYPR-CD00055

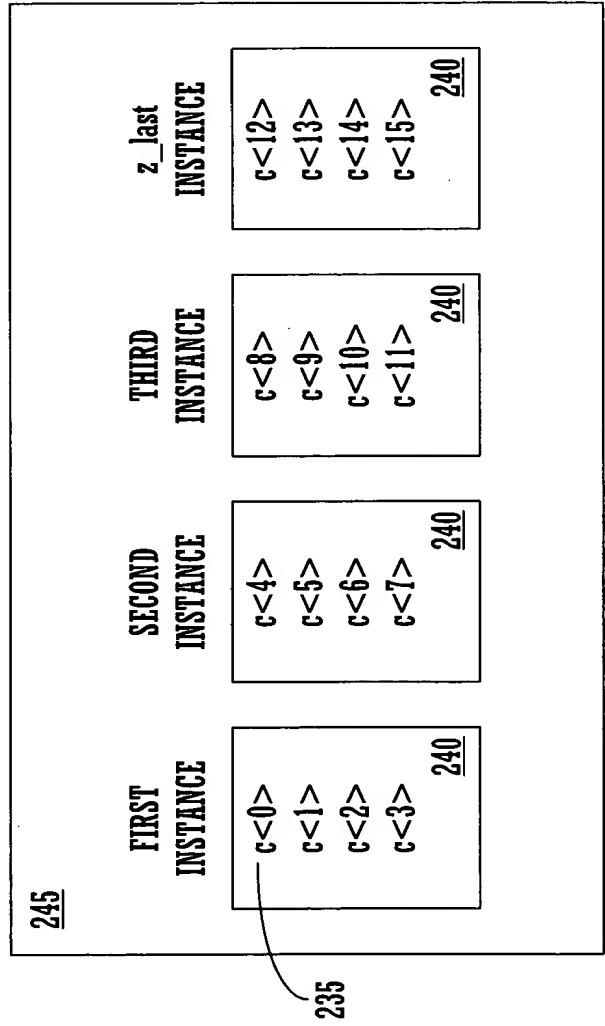


FIGURE 2B

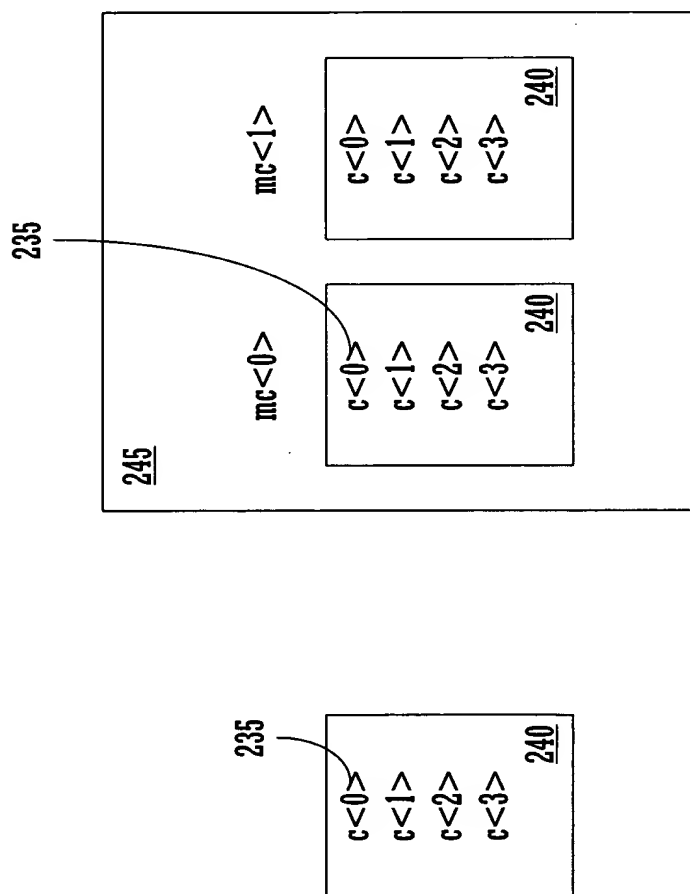


FIGURE 2C

TITLE: METHOD AND SYSTEM FOR GENERATING A BIT ORDER DATA STRUCTURE OF
CONFIGURATION BITS FROM A SCHEMATIC

INVENTOR(S): James Daniel Merchant, Gordon Carskadon, Brian P. Evans, Jeffrey Scott Hunt, Anup Nayak,
Andrew Wright

USSN: 09/684,160 ATTORNEY DOCKET #: CYPR-CD00055



6/16

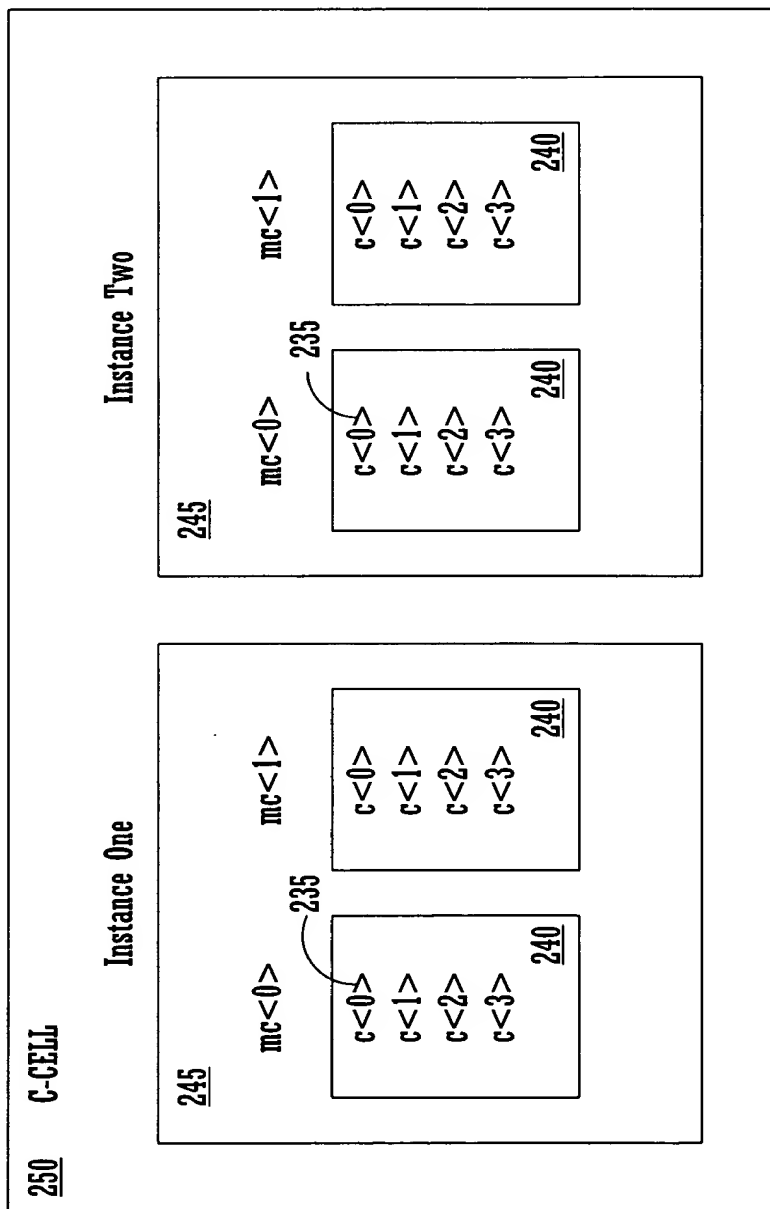


FIGURE 2D

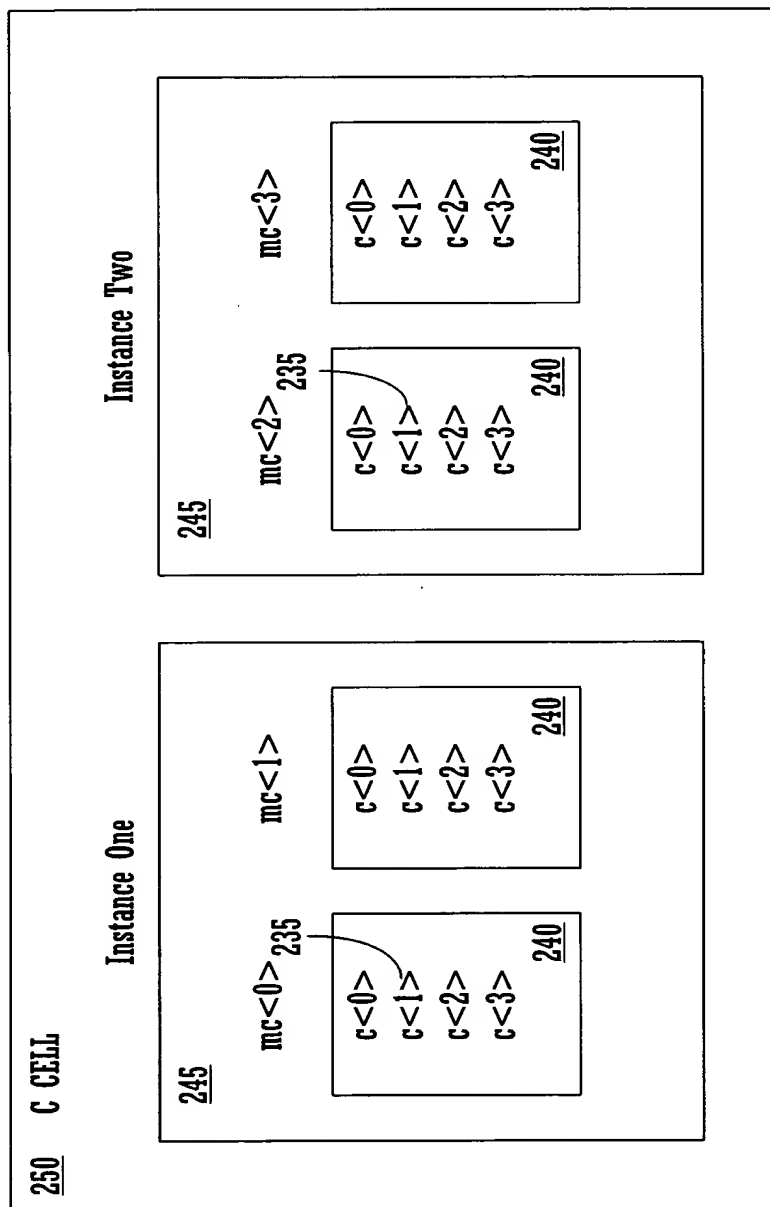


FIGURE 2E



8/16

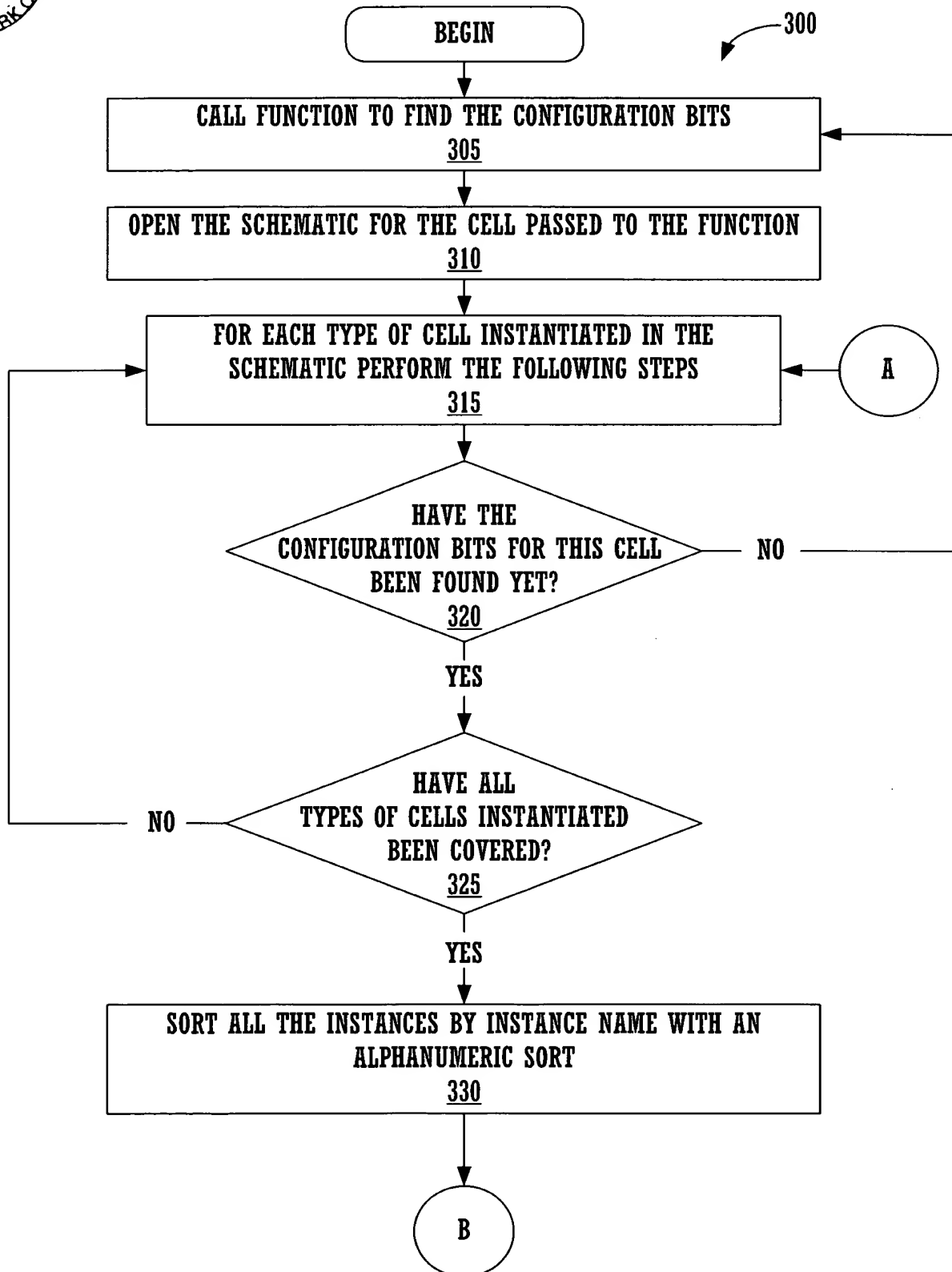


FIGURE 3A

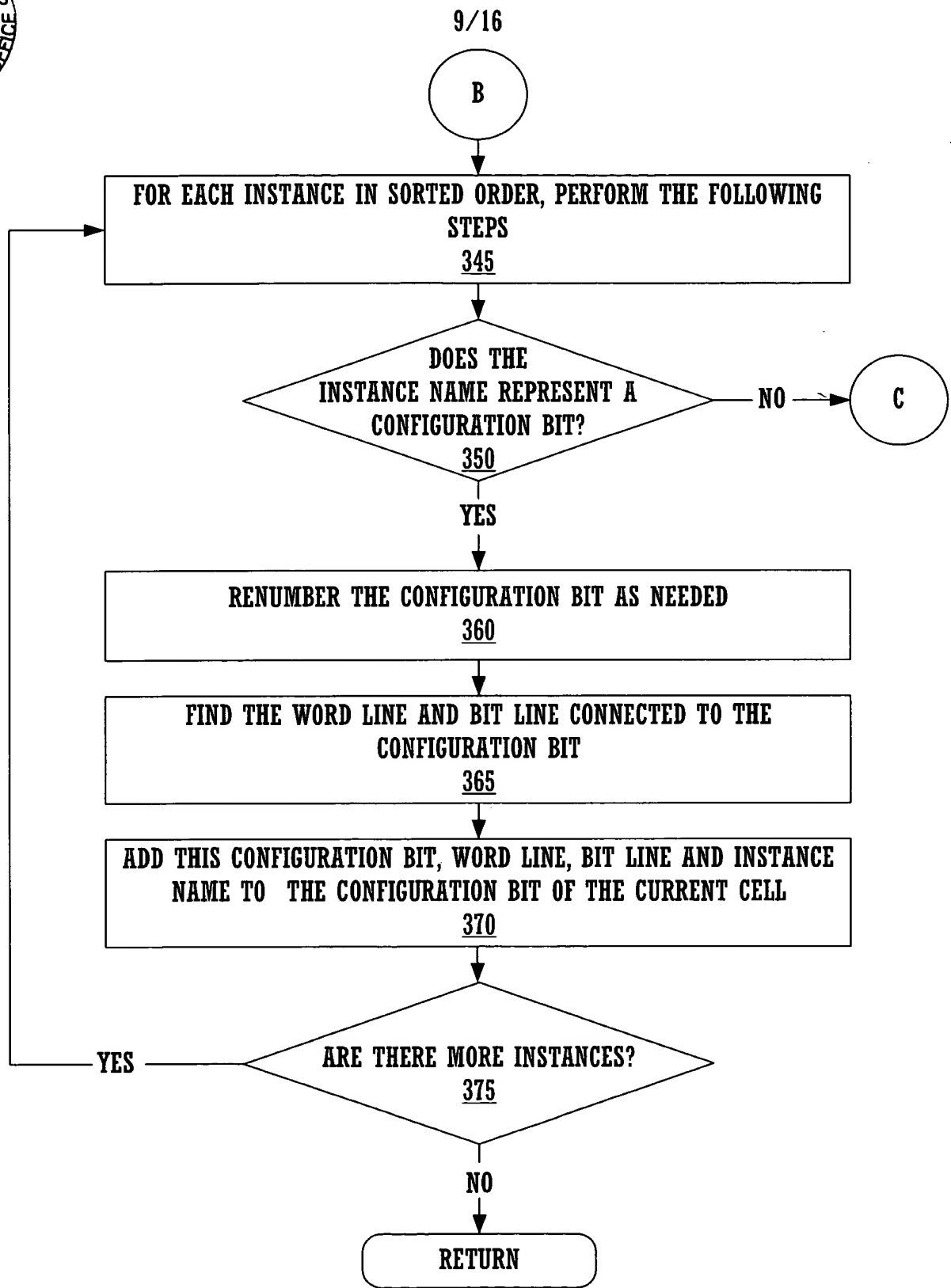


FIGURE 3B

10/16

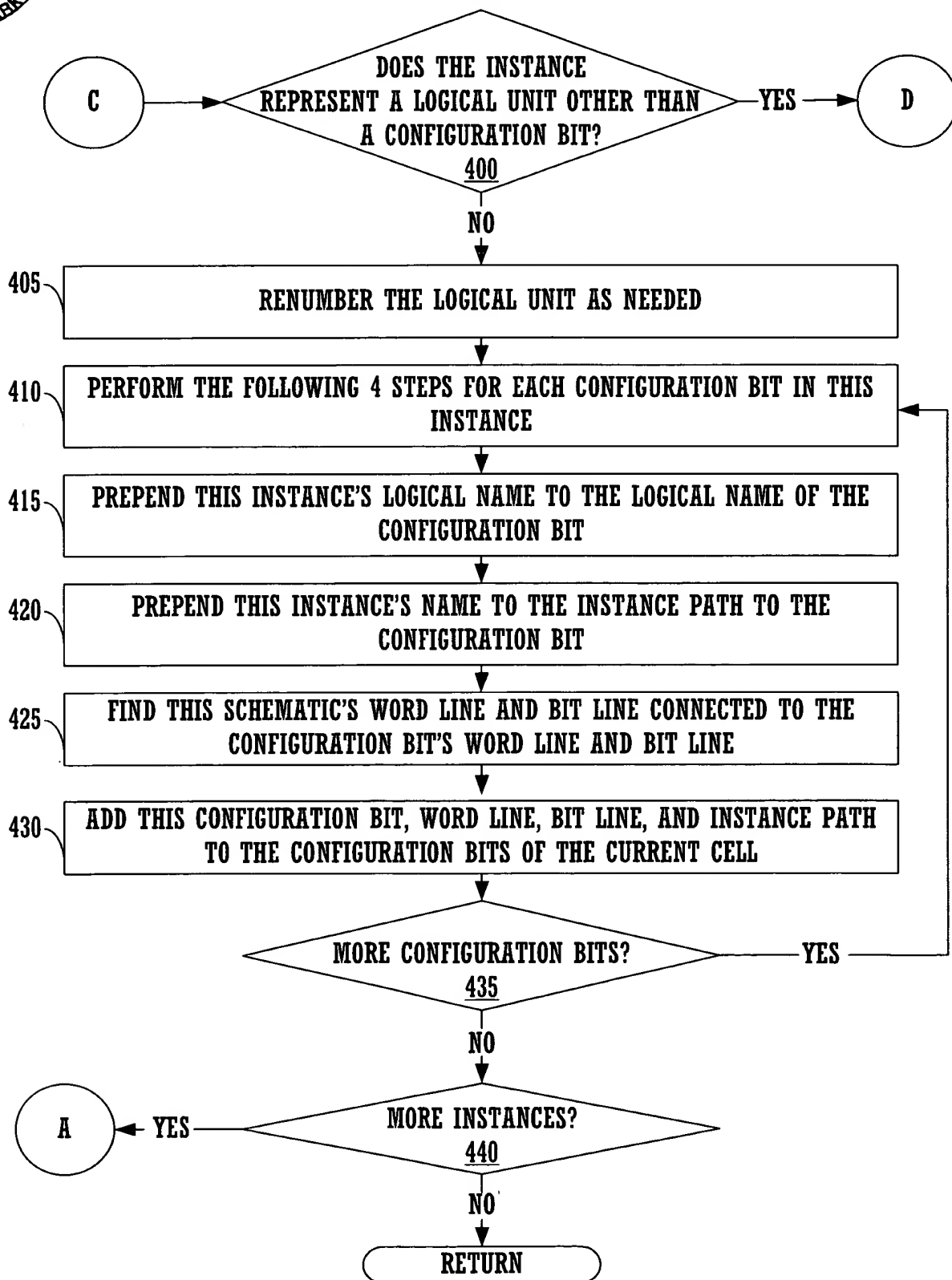
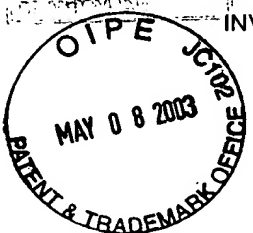
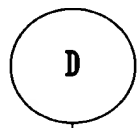


FIGURE 3C



11/16



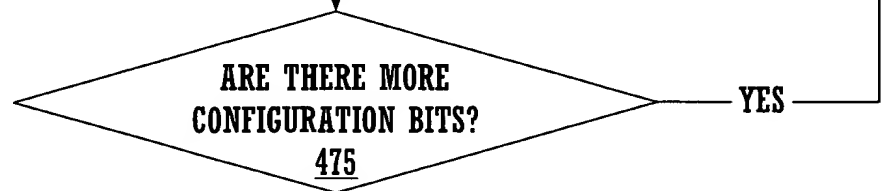
FOR EACH CONFIGURATION BIT IN THIS INSTANCE PERFORM THE FOLLOWING STEPS
450

RENUMBER THE CONFIGURATION BIT AS NEEDED
455

PREPEND THIS INSTANCE'S NAME TO THE INSTANCE PATH TO THE CONTROL PATH
460

FIND THIS SCHEMATIC'S WORD LINE AND BIT LINE CONNECTED TO THE CONFIGURATION BIT'S WORD LINE AND BIT LINE
465

ADD THIS CONFIGURATION BIT, WORD LINE, BIT LINE AND INSTANCE PATH TO THE CONFIGURATION BITS OF THE CURRENT CELL
470



RETURN

FIGURE 3D

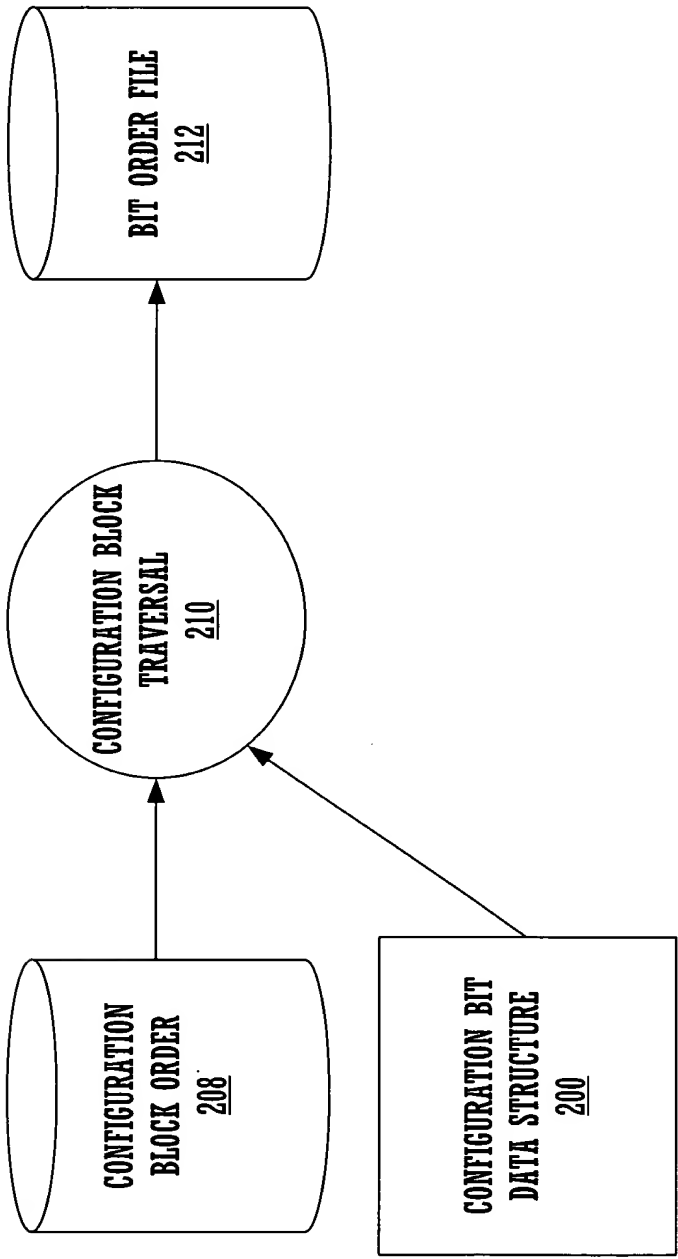


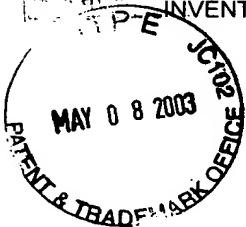
FIGURE 4A

FIG. 1
BY
E

TITLE: METHOD AND SYSTEM FOR GENERATING A BIT ORDER DATA STRUCTURE OF
CONFIGURATION BITS FROM A SCHEMATIC

INVENTOR(S): James Daniel Merchant, Gordon Carskadon, Brian P. Evans, Jeffrey Scott Hunt, Anup
Nayak, Andrew Wright

USSN: 09/684,160 ATTORNEY DOCKET #: CYPR-CD00055



13/16

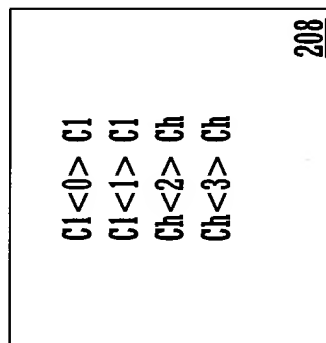


FIGURE 4B

```
254— begin c1 188 422
256— 1b<0>/mc<0>/c<0>
256— 1b<0>/mc<0>/c<1>
256— 1b<0>/mc<0>/c<2>
      spacer 8
      endWordLine 0
256— 1b<0>/mc<1>/c<0>
256— 1b<0>/mc<1>/c<1>
256— 1b<0>/mc<1>/c<2>
      spacer
      endWordLine 1
256— cm<1>/crcfg<2>/c<0>
256— cm<1>/crcfg<2>/c<1>
256— cm<1>/crcfg<2>/c<2>
256— cm<1>/crcfg<2>/c<3>
258 end c1
260 inst c1 c100 0 0
260 inst c1 c101 0 1
260 inst c1 c102 0 2
260 inst c1 c103 0 3
260 inst c1 c110 1 0
```

FIGURE 4C

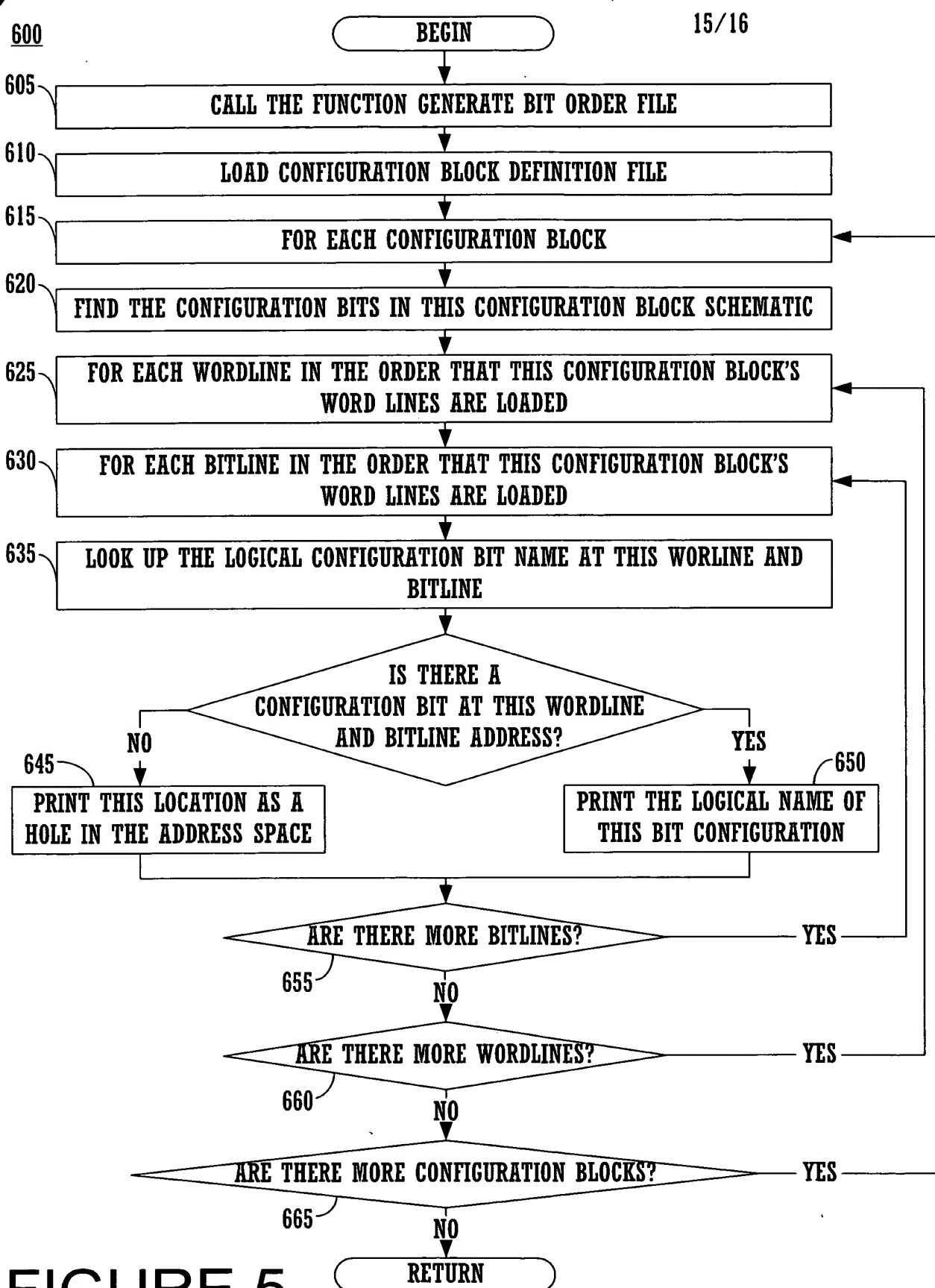


FIGURE 5



16/16

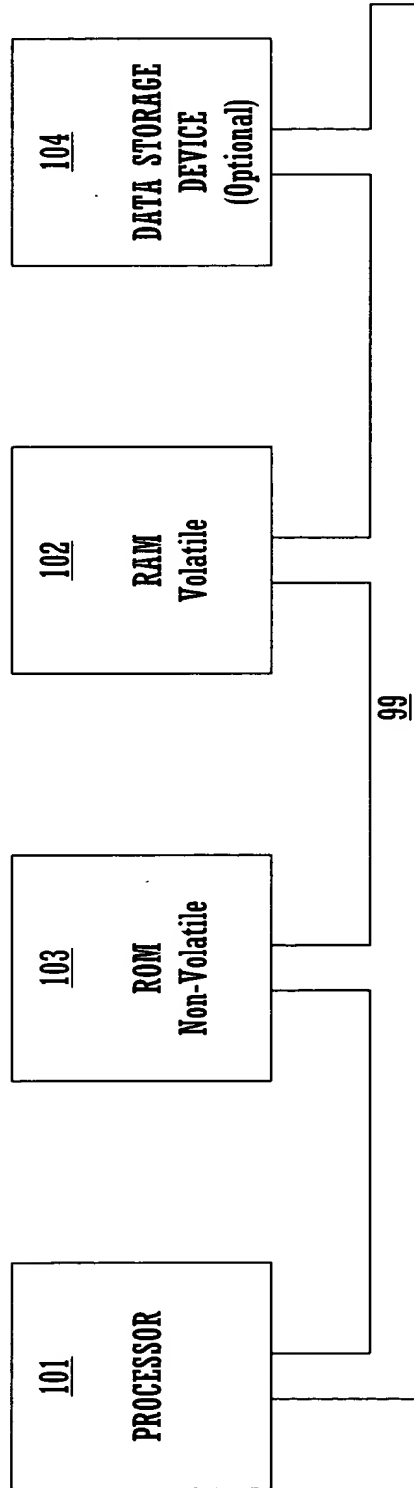


FIGURE 6